Nanometer Scale Lithography of Silicon and Titanium using Scanning Probe Microscopy

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Abstract

This paper reports on the fabrication of nanometer-resolved oxide patterns on titanium and silicon by Scanning Probe Microscopy (SPM). The dimensional characteristics of thin oxide lines are studied as a function of the anodisation voltage and writing velocity. Examples of direct patterning of single electron transistors (SET) and single electron memory (SEM) potentially operating at room temperature is also given to illustrate the potential and flexibility of lithography based on Tapping-Mode Atomic Force Microscopy (TM-AFM).

I- Introduction

Low energy scanning probe microscopy (SPM) has recently attracted much attention for its potential to produce patterns with ~10 nm lateral resolution. Nanometer-sized features have been successfully defined using exposure of resists [1], decomposition of organometallic compounds [2] or selective oxidation of hydrogenated silicon [3] and amorphous silicon [4]. Recently, direct formation of oxide barriers has been demonstrated on a thin titanium film using a scanning tunneling microscope (STM) [5]. In addition, titanium can be deposited on almost any surface while titanium dioxide can be used as a masking level for dry and chemical etching steps. These properties can be used to extend the application field of SPM-based lithography when nano-patterning of isolating layers (e.g. SiO_2) is needed in silicon technology. This paper reports the fabrication of nanometer-resolved oxide patterns on silicon and titanium by scanning tunneling microscopy (STM) and atomic force microscopy in tapping mode (TM-AFM). The dimensional characteristics of thin oxide lines are studied as a function of the anodisation voltage and writing velocity. Examples of direct patterning of single electron transistors (SET) and single electron memory (SEM) potentially operating at room temperature is also given to illustrate the potential and flexibility of lithography based on TM-AFM.

II- Experiments and results

Fig. 1 shows an example of STM-based nano-oxidation of silicon performed in air. Sub-10 nm can be achieved using this technique. However, STM suffers from the impossibility to decouple the anodisation bias from the tip-sample separation. In addition, degradation of the tip can occur both in imaging and lithography modes when scanning over high resistivity regions (e.g. tip crash into oxide).

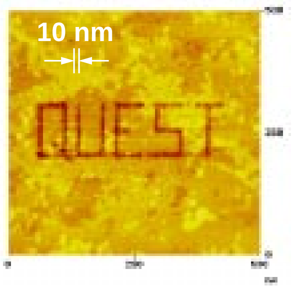

Fig. 1: Nano-oxidation of Silicon (111) using STM (bias 3 V, current 20 pA, tip speed 1µm/s)

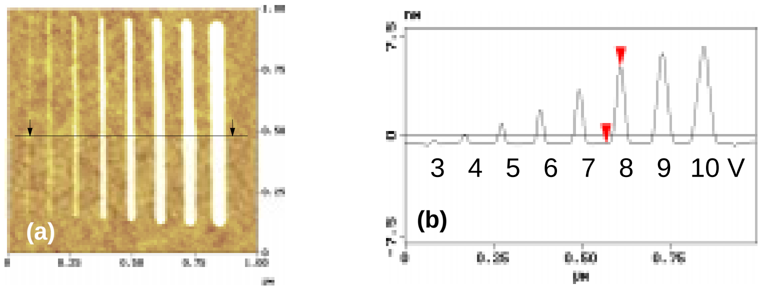

Fig. 2: Nano-oxidation of Titanium using TM-AFM
Sensivity of the oxide height to the anodisation voltage
a) TM-AFM image b) anodic oxide profile along cross-section defined in a) (tip velocity 0.1 mm/s, cantilever amplitude of vibration 4 nm, 9 nm thick titanium film)

In contrast, AFM holds a distinct advantage over STM because the exposure mechanism, typically an electric field, can be applied independently of the feedback control that governs the tip-sample spacing. In addition, tapping-mode AFM eliminates lateral shear forces and overcomes tip-sample adhesion forces (e.g. capillarity). These properties avoid damages on the surface and improve imaging and lithography resolution. Fig. 2 reports the sensivity of the height of oxide lines as a function of the anodisation voltage applied to a thin titanium film. Fig. 3 shows the logarithmic dependence of the height of oxide line produced on a titanium film for an increasing writing velocity. The observed dependences of the oxide height with the anodisation voltage (linear) and tip velocity (logarithmic) can be explained by the field-assisted oxidation theory of very thin metal films [6].

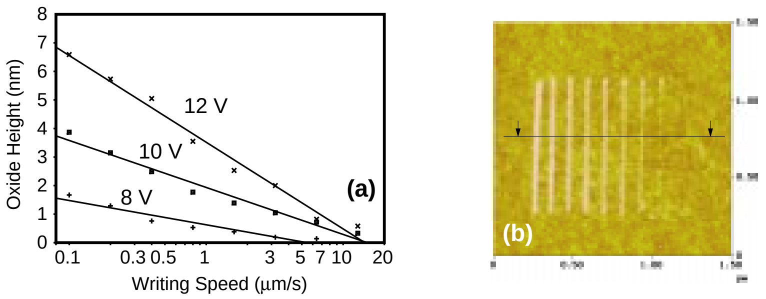

Fig. 3: Nano-oxidation of Titanium using TM-AFM
a) Sensivity of the oxide height to the tip velocity for different anodisation voltages b) TM-AFM image of oxide lines with following conditions: (anodisation bias 10 V, cantilever amplitude of vibration 4 nm, 9 nm thick titanium film)

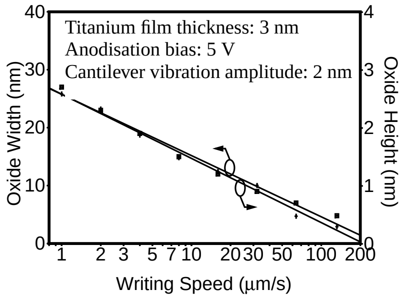

Fig. 4: Nano-oxidation of Titanium using TM-AFM - Sensivity of the oxide height and width to the tip velocity (constant height/width ratio)

Fig. 4 reports the variations of the height and width of the oxide patterns on titanium as a function of the tip velocity. The same kinetic law holds for lateral oxidation and the line width that determines the lateral resolution is found proportional to the oxide height. Because field-assisted oxidation can also produce thick and large insulating barriers in a single tip pass, gate to channel isolation can be performed with the same technique that allows for the formation of thin tunnel barriers.

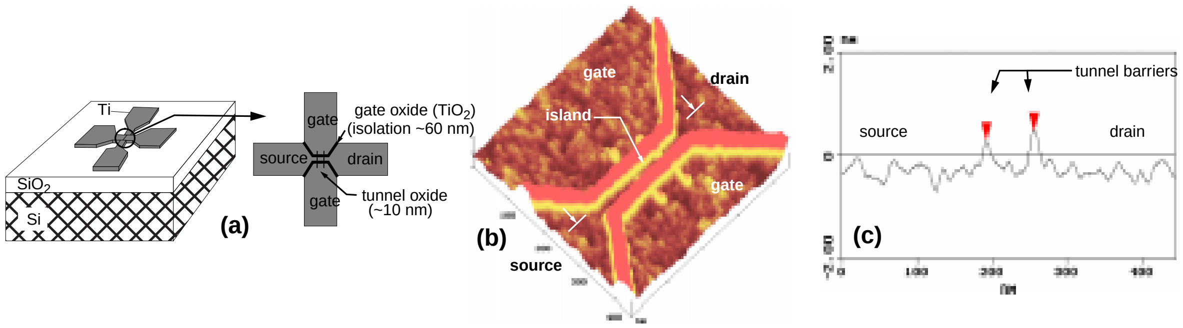

Fig. 5: Direct formation of a single electron transistor on Titanium (gate oxide and tunnel oxide barriers by oxidation of a thin Ti film: 4 nm) a) layout of a region including contact pads where Ti is lifted-off using optical lithography. TM-AFM based nano-oxidation is used to pattern a SET in the central area
b) TM-AFM image c) height profile along the channel as defined in b)
(anodisation voltage 5 & 6 V, tip velocity 3 & 0.1 μm/s, cantilever amplitude of vibration 20 nm)

Fig. 5 shows a possible implementation of a SET with in-plane gates for which thin and thick oxide barriers are defined on a thin titanium film. Another potential application of this technique is the single electron memory which is exemplified in Fig. 6.

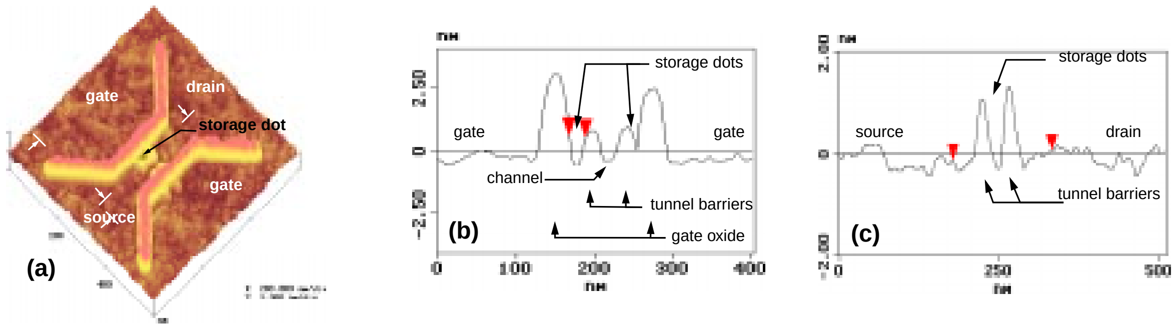

Fig. 6: Direct formation of an single electron memory on Titanium (gate oxide and tunnel oxide barriers by oxidation of a thin Ti film: 4 nm) a) TM-AFM image b) height profile across the channel c) profile parallel to the channel direction and intercepting a storage dot (anodisation voltage 5 & 6 V, tip velocity 3 & 0.1 μm/s, cantilever amplitude of vibration 20 nm)

Beyond the direct formation of insulating barriers, anodic oxide obtained by SPM also offers excellent resistance to selective wet or RIE etching. Fig. 7 shows an array of 16 dots produced on silicon using TM-AFM oxidation and subsequently etched using RIE (SF_6). This type of feed gaz offers sufficent anisotropy and high selectivity to etch 40 nm of Si starting from a SiO_2 mask as thin as 1 nm. SPM-based nano-lithography of polysilicon is more challenging when performed on substrates with large initial roughness or with granular morpholy (e.g. polysilicon). However, Fig. 8 demonstrates that excellent pattern transfer is again obtained when oxide generated using AFM is combined to selective dry etching.

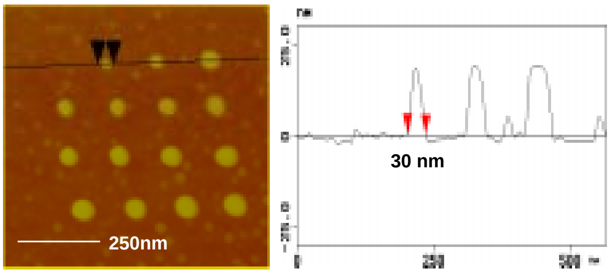

Fig. 7: Top-view and cross-section of an array of 16 oxide dots produced by TM-AFM on Silicon and subsequently etched with SF_6 plasma (pressure 50 mTorr, RF power 30W, duration 6s).

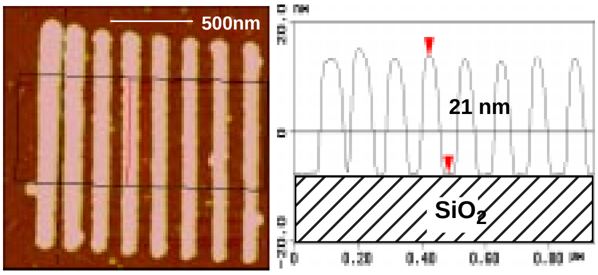

Fig. 8: Top-view and cross-section of 8 oxide stripes produced by CM-AFM on α-silicon and subsequently etched with SF_6 plasma (pressure 50 mTorr, RF power 30W, duration 5s).

III- Conclusion

SPM-based oxidation offers high potential for solving nanometer-scale lithography problems that conventionnal techniques can hardly handle. The best candidate clearly appears to be tapping-mode AFM as it retains the resolution performance of STM (in air) for the generation of oxide patterns due to the soft interaction between surface and tip.

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